REMARKS

This application has been carefully reviewed in light of the office action mailed July 11, 2003. Claims 1-20 are pending in this application. Applicant respectfully requests early and favorable acceptance of this application.

35 U.S.C. § 102 Rejections

Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Digabel, U.S. Patent No. 6,138,029. Applicant respectfully traverses the rejection.

The Digabel reference discloses a smart card reader containing first and second oscillators OSC1 and OSC2 that produce clock signals Clk1 and Clk2, respectively, at inputs of a multiplexer MX contained in a switching device SW. Multiplexer MX selects between Clk1 and Clk2 based on the value of a control signal Cmd, thereby producing a signal CLK at a clock terminal of the card reader. A phase detector PD determines the phase relationship between Clk1 and Clk2 and enables a latch L3 that enables MX to switch only when Clk1 and Clk2 have quasi-simultaneous edges, thereby avoiding a the presence of an unwanted active edge in CLK.

Claim 1

Claim 1 recites a smart card reader (e.g., 8) that includes, among other features, a detection circuit (e.g., 26) with a plurality of inputs (e.g., 30, 38, 42) for monitoring a plurality of operating conditions, and a plurality of outputs (e.g., 53-56) for providing a plurality of sense signals (e.g., VCCOK, VCCOC, VBATOK, CRDINS). A multiplexer (e.g., 60) receives a selection

signal (e.g., ADDR) for routing one of the sense signals to an output as a status signal (e.g., STATUS).

The reference does not disclose, teach or fairly suggest a detection circuit for monitoring a plurality of operating conditions of a card reader and has a plurality of outputs for providing a plurality of sense signals. Two of the inputs to the Digabel multiplexer MX receive clock signals Clk1 and Clk2, neither of which can reasonably be construed as a sense signal. Moreover, Clk1 and Clk2 are produced by OSC1 and OSC2, respectively, neither of which is disclosed as operating as a detection circuit that monitors an operating condition as claimed. A third input to the Digabel multiplexer MX receives, through latch L3, an enable signal En produced by phase detector PD when edges of Clk1 and Clk2 are quasi-aligned. However, even if the Clk1-Clk2 phase alignment in the Digabel reference were deemed an operating condition of a card reader and phase detector PD is construed as a detection circuit, PD has only one output that produces one signal, not a plurality of outputs producing a plurality of sense signals as claimed.

Accordingly, it is respectfully submitted that claim 1 is not anticipated by the Digabel reference.

Claims 2-7 depend from claim 1 and should be allowable for at least the same reasons as claim 1.

Claim 8

Claim 8 recites an integrated circuit (e.g., 10) for controlling a smart card (e.g., 15), including, among other features, a monitoring circuit (e.g., 26) having first and second inputs (e.g., 38, 30) for monitoring first and second operating conditions of the integrated circuit to produce first and second sense signals (e.g., VCCOK, VBATOK) at first and second outputs (e.g., 53, 55), respectively.

For at least the reasons discussed in conjunction with claim 1 above, the Digabel reference does not disclose a monitoring circuit whose first and second inputs monitor first and second operating conditions to produce first and second sense signals at first and second outputs. Phase detector PD has only one output producing one signal En, not first and second outputs producing first and second sense signals as claimed.

Accordingly, it is respectfully submitted that claim 8 is not anticipated by the Digabel reference.

Claims 9-13 depend directly or indirectly from claim 8 and should be allowable for at least the same reasons as claim 8.

Claim 14

Claim 14 includes, among other features, monitoring first and second operating conditions of the card reader to produce first and second sense signals, respectively; selecting between the first and second sense signals with a selection signal to produce a status signal

For reasons similar to those discussed in conjunction with claim 1 above, the Digabel reference does not disclose the steps of monitoring first and second operating conditions to produce first and second sense signals. Phase detector PD has only one output producing one signal En, not first and second outputs producing first and second sense signals as claimed. Further, Digbel does not and can not disclose the additional step of selecting between the first and second sense signals with a selection signal to produce a status signalSince the Digabel reference only discloses the one output, it can not select between two sense signals. Accordingly, it is respectfully submitted that the Digabel reference does not anticipate claim 14.

Claims 14-20 depend directly or indirectly from claim 14 and

should be allowable for at least the same reasons as claim 8.

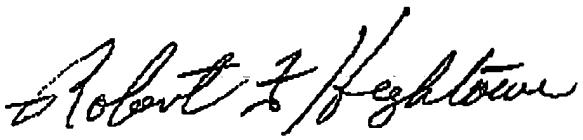
CONCLUSION

Applicant has made an earnest attempt to place this case in condition for allowance. In light of the remarks set forth above, Applicant respectfully requests reconsideration and allowance of claims 1 - 20.

While no fees are believed due, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account 50-1086.

If there are matters which can be discussed by telephone to further the prosecution of this Application, Applicant invites the Examiner to call the undersigned attorney/agent at the Examiner's convenience.

Respectfully submitted,
Dominique Omet



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